REMARKS

Claims 1, 3-5, 7, 8, 11 and 14-22, 24-33 and 35-41 are now presented for examination. Claims 1, 11, 21, 22, 27, 30-33, 38 and 41 have been amended to define still more clearly what Applicant regards as his invention. Claims 23 and 34 have been cancelled without prejudice. Corrected formal drawings are submitted herewith to make the changes approved by the Examiner in the Office Action of November 29, 1993. Claims 1, 11 and 31 are the only independent claims.

Applicant notes with appreciation the indication that Claim 1, and presumably the claims dependent thereon, would be allowable if rewritten so as to overcome the formal rejection discussed below. In view of the discussion regarding Claim 1 below, those claims are now believed to be in condition for allowance.

Claims 11 and 21-41 were rejected under Section 112, first paragraph as allegedly not supported by the specification, which was objected to for the same reasons.

Our file notes also indicates that prior to issuance of the most recent Office Action in the parent application, in a November 4, 1993 telephone conversation with Mr. Jack Cubert of our office the Examiner proposed the above amendments to Claims 11, 21, 22, 27, 30-33, 38 and 41. According to the Examiner, the amendments would have brought the application in condition for allowance, and made those claims more clearly correspond to Figure 15. After Applicant approved of the amendments, the Examiner stated in a telephone conversation that he would enter them by Examiner's amendment. However, the Examiner instead issued the Office Action dated November 29, 1993, which was based upon the claims as they stood without having entered the proposed amendments. Thus, the proposed amendments are being submitted here for the first time. Our file notes

also indicate that submission of the amendments in response to the Office Action was suggested by the Examiner in a telephone conversation with Mr. Cubert dated November 12, 1993, the same telephone conversation in which the Examiner informed Applicant's attorney that he would issue a new Office Action.

With regard to the rejections based on Section 112, first paragraph, as to the recitations of Claims 11 and 31 objected to in the Office Action, the above amendments to those claims are believed to obviate the Section 112, first paragraph, rejections. As amended, in the manner suggested by the Examiner, Claims 11 and 31 are believed to be fully supported, for example, by Figure 15.

As to the rejections of Claims 27 and 38, relating to the impurity concentration not being greater than 10^{17} cm^{-3}, in view of the amendments to those claims, as well as the amendment to their respective base claims, and the similar recitation of the impurity concentration in *originally-filed* Claim 16 (which is considered part of the original disclosure for support purposes), it is believed clear that amended Claims 27 and 38 are supported.

The rejections of Claims 22 and 33 are believed obviated by the amendments to those claims as well as the amendments to their base claims. As to the comments in the Office Action appearing at the top of page 3, it is not clear how those comments relate to Claims 22 and 33. Accordingly, they cannot form the basis of a rejection regarding those claims.

Cancellation of Claims 23 and 34 renders their rejections moot.

Claims 1, 3-5, 7, 8 and 14-20 were rejected under 35 U.S.C. § 112, second paragraph, as indefinite. In particular, the position was taken in the Office Action that it

was unclear what an "electrically neutral area" is. An electrically neutral area is an area in which carriers are excluded, as in the vicinity of the interface between the gate insulation film and the semiconductor, to prevent irregularities at the interface. See the specification at page 26, lines 17-22 and page 10, lines 24-25. It is believed that the rejection under Section 112, second paragraph, has been obviated, and its withdrawal is therefore respectfully requested.

OK

In view of the foregoing amendments and remarks, and in view of the long delay caused by the Office losing this file, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

Applicant's undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,

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MARKED-UP VERSION SHOWING THE CHANGES MADE TO THE CLAIMS

Claims 1, 11, 21, 22, 27, 30-33, 38 and 41 have been amended as follows:

1. (Twice Amended) A semiconductor device provided at least with [a semiconductor layer including] source and drain regions of a first [conductive] conductivity type and a semiconductor layer including a channel region between said source and drain regions, an insulating layer covering at least said channel region, and a gate electrode arranged close to said insulating layer,

wherein said channel region comprises a first channel area of a second conductivity type opposite to the first conductivity type and of low resistivity arranged close to said insulating layer, a second channel area of the first conductivity type and of a high resistivity arranged close to said first channel area, and a third channel area of the second conductivity type arranged close to said second channel area, said third channel area is arranged close to an additional insulating layer, and an electrically neutral area is formed in said third channel area at a side adjacent to said additional insulating area.

11. (Twice Amended) A semiconductor device provided at least with a semiconductor layer including source and drain areas of a first conductive type and of a high impurity concentration and a channel area positioned between said source and drain areas, an insulation layer covering at least said channel area, and a gate electrode positioned close to said insulation layer, wherein said channel area at least comprises a first

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wherein said channel region comprises a first channel area of a second conductivity type opposite to the first conductivity type and of low resistivity arranged close to said insulating layer, a second channel area of the first conductivity type and of a high resistivity arranged close to said first channel area, and a third channel area of the second conductivity type arranged close to said second channel area, said third channel area is arranged close to an additional insulating layer, and an electrically neutral area is formed in said third channel area at a side adjacent to said additional insulating area.

11. (Twice Amended) A semiconductor device provided at least with a semiconductor layer including source and drain areas of a first conductive type and of a high impurity concentration and a channel area positioned between said source and drain areas, an insulation layer covering at least said channel area, and a gate electrode positioned close to said insulation layer, wherein said channel area at least comprises a first

channel area of a low resistance, positioned close to said insulation layer and having a second conductive type opposite to said first conductive type, and a second channel area of a high resistance, having said first conductive type and positioned adjacent to said first channel area, and [wherein said channel area] further comprises a [third channel area] substrate of the second conductive type, positioned adjacent to said second channel area, said semiconductor device constituting an integrated circuit including an MIS transistor comprising a [fourth] third channel area of the first conductive type having an impurity concentration different from the second channel area, positioned between the first and second channel areas.

21. (Amended) A semiconductor device according to claim 11, wherein the impurity concentration of said [fourth] third channel area is higher than that of said second area.

22. (Amended) A semiconductor device according to Claim 11, wherein the impurity concentration of said [fourth] third channel area is lower than that of said second area.

23. (Cancelled).

27. (Amended) A semiconductor device according to Claim 11, wherein the impurity concentration in said second or [fourth] third channel area is not greater than 10^{17} cm^{-3}.

30. (Amended) A semiconductor device according to Claim 11, wherein the impurity concentration in said [third channel area] substrate is 10^{14}-10^{18} cm^{-3}.

31. (Amended) A semiconductor device provided at least with source and drain regions of a first conductivity type and of a high impurity concentration, a semiconductor layer including a channel region between said source and drain regions, an insulating layer at least on said semiconductor layer, and a gate electrode on said insulating layer, wherein at least said semiconductor layer comprises a first area of low resistivity and of a second conductivity type opposite to the first conductivity type adjacent to said insulating layer, a [fourth] third area of the first conductivity type, having an impurity concentration different than the second channel area, adjacent to the first area, a second area of the first conductivity type adjacent to said [fourth] third area, and a [third channel area] substrate of the second conductivity type adjacent to said second area.

32. (Amended) A semiconductor device according to claim 31, wherein the impurity concentration of said [fourth] third area is higher than that of said second area.

33. (Amended) A semiconductor device according to Claim 31, wherein the impurity concentration of said [fourth] third area is lower than that of said second area.

34. (Cancelled).

38. (Amended) A semiconductor device according to Claim 31, wherein the impurity concentration in said second or [fourth] third area is not greater than 10^{17} cm^{-3}.

41. (Amended) A semiconductor device according to Claim 31, wherein the impurity concentration in said [third area] substrate is 10^{14}-10^{18} cm^{-3}.